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Active Low Pass Filter based Efficient DC-DC Converter

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Abstract

In An efficient active filter based on-chip DC-DC voltage converter circuit is proposed which is used for application to distribute power supplies in multivoltage system. The circuit is appropriate for point-of-load voltage regulation due to an ultra area efficient architecture. Compare to other conventional voltage regulators, the proposed circuit is designed with small area and with no inductor or output capacitor. This is an alternative to classical LDO voltage regulators and hence, providing a means for distributing multiple local power supplies across an integrated circuit while maintaining high efficiency and fast response time within a small area. Thus, the performance of proposed active filter based DC-DC converter is analysed.

Keywords: Active filter, Buck converter, Op-Amp, Point-of-load voltage regulation

Introduction

The power supply voltage aggressively scales with each technology generation, making the delivery of a high quality supply voltage to noise sensitive circuit blocks highly challenging. Moreover, supply voltage is sometimes tuned in time to achieve lower power consumption, which is called dynamic voltage scaling. The supply of many different and dynamically scaled voltages from outside the package gives rise to much overhead in area. The power line integrity, including IR drop and noise, becomes an issue as well. The distributed on-chip power supply circuits are useful for solving these problems. High voltage is distributed by a main power grid and is then converted to the lower voltages at the vicinity of the target blocks by distributed on-chip voltage converters. This approach reduces cost and power integrity issues.

For dc–dc converters, linear regulator, buck converters and switched capacitor converter are well known circuits. A buck converter is a standard switching dc–dc converter circuit topology with high efficiency and good output voltage regulation characteristics. [5]But it requires large passive elements of inductance and capacitance (*LC*) for an output filter but it shows a higher power efficiency than a linear regulator. A switched-capacitor converter also needs large capacitors and one more drawback is that the output voltage levels are limited by the ratios of prepared capacitors. That is not very suitable for low-power dynamic voltage scaling systems.[6]

A more area efficient voltage converter structure is a low dropout voltage regulator (LDO) [7]–[14]. These regulators are implemented on-chip close to the load circuitry for fast and accurate load regulation. These regulators require a large output capacitance to achieve fast load regulation. This capacitor occupies significant on-chip area and is therefore generally implemented off-chip. The off-chip implementation of the output capacitor requires dedicated I/Os and produces higher parasitic losses. Alternatively, when the output capacitor is placed on-chip, the output capacitor dominates the total LDO regulator area [9]. Many techniques have been proposed to eliminate the need for the large off-chip capacitor without sacrificing the stability and performance of an LDO regulator. Due to the large area requirement, LDO regulators are not appropriate for a system of distributed point-of-load voltage regulators.

To produce a voltage regulator appropriate for distributed point-of-load voltage generation, the passive LC filter within a buck converter is replaced with a more area efficient active filter circuit [16]–[19]. A switching input voltage is used to generate the desired output voltage, and the converter uses a filter

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structure to produce the desired output voltage. The current supplied to the output node, however, does not originate from the input switching signal, rather, it originates from the operational amplifier (Op Amp) output stage, similar to a linear voltage converter. The proposed voltage converter is therefore a hybrid combination of a switching and linear DC–DC converter. The on-chip area of the proposed hybrid regulator is 0.015mm^2, which is significantly smaller than state-of-the-art output capacitor less LDOs. The power efficiency, however, is limited to *V*out/*V*in, similar to an LDO.

This paper is organized as follows. Section II reviews the existing conventional buck converter. Section III describes the active filter based buck converter design and its performance analysis. Section IV concludes the paper.

Existing Conventional Voltage regulator

A switching DC-DC converter generating an output voltage lesser than the input supply voltage is called buck converter is shown in Fig.1. The passive inductor and capacitor are generally implemented off-chip due to the significant on-chip area required by these elements. The PMOS and NMOS drive transistors generate a switching signal at Node1, shown in Figure. 1(a). The low pass LC filter removes the high frequency harmonics of the switching signal, and generates

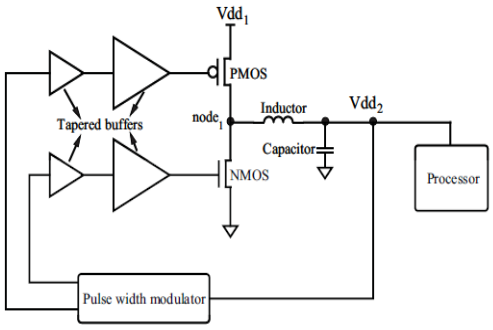
$Vdd_2(t) = Vdd_2 + Vr(t)$ (1)

where Vdd_2 is the output dc voltage and Vr is the output voltage ripple due to the non ideality of the low pass filter. Vdd_2 is the average value of the switching voltage at Node1, which is

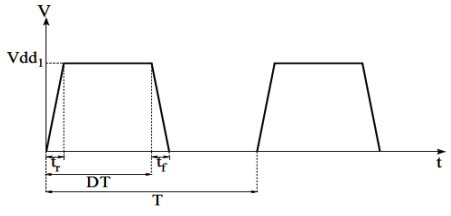
$$Vdd_2 = Vdd_1 \left(D - \frac{tr-tf}{2T} \right) \quad (2)$$

where D, tr, tf and T are, respectively, the duty cycle, rise time, fall time, and period of the switching voltage as illustrated in Fig. 1(b). When the rise and fall times of the switching signal are the same, the output voltage is

$Vdd_2 = D\ Vdd_1$ (3)



(a)



(b)

Figure.1 Conventional buck converter. (a) Buck converter where the inductor and capacitor are typically implemented off-chip due to the large area. (b) Signal waveform at the output of the power MOSFETs (node1) where D, tr, tf and T are, respectively, the duty cycle, rise time, fall time, and period of the switching voltage.

The amplitude of the ripple voltage depends on both the filter characteristics and the variation of the output current demand. The amplitude of the ripple voltage becomes larger for a finite time when the output current demand changes abruptly. Additionally, the pulse width modulator (PWM), shown in Figure.1, can be programmed to generate a different duty cycle to vary the output dc voltage.

Active Low Pass Filter based DC-DC Converter Design

In the proposed circuit, the LC filter is replaced by active filter and the large buffers are replaced by small buffers in order to gain small die area. The switching input signal generated at Node1 is filtered by the active filter structure, similar to a buck converter, and a dc voltage is generated at the output. Increasing the duty cycle D of the input switching signal at Node1 increases the generated dc voltage as shown in Figure.2.

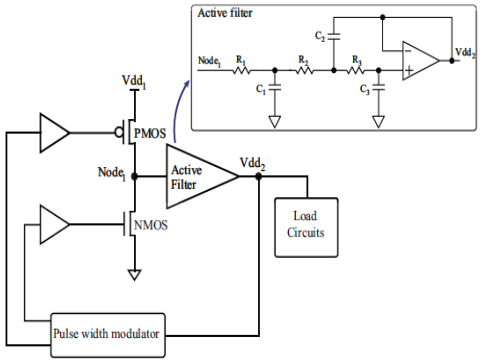


Figure.2 Proposed DC–DC converter. Note that the passive LC filter is replaced with an active filter and the large tapered buffers are no longer necessary

Large tapered buffers are required in a conventional buck converter to drive the large power

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transistors, PMOS and NMOS, as shown in Figure. 2. The current delivered to the load circuitry is provided by these large power transistors. In the proposed circuit, however, the current delivered to the load circuitry is supplied by an Op Amp. Small buffers are therefore sufficient for driving the active filter. Replacing the tapered buffers with smaller buffers significantly decreases the power dissipated by the input stage. Alternatively, the output buffers within the Op Amp dissipate power within the regulator.

Another characteristic of the regulator is that the feedback required for line and load regulation is satisfied with separate feedback paths, as shown in Figure. 2. Feedback1 is generated by the active filter structure and provides load regulation, whereas feedback2 is optional and controls the duty cycle of the switching signal for line regulation. In most cases, feedback1 is sufficient to guarantee fast and accurate load regulation. When only one feedback path is used, the switching signal is generated by simpler circuitry (e.g., a ring oscillator) and the duty cycle of the switching signal is compensated by a local feedback circuit (a duty cycle adjustor). The primary advantage of a single feedback path is the smaller area since feedback1 is produced by the active filter and no additional circuitry is required for the compensation structure.

A. Active Filter

Active filter is usually used for output voltage stabilization of DC/DC converters. Active filter structures contain no passive inductors. The filtering function uses capacitors, resistors, and an active circuit (i.e., the Op Amp).

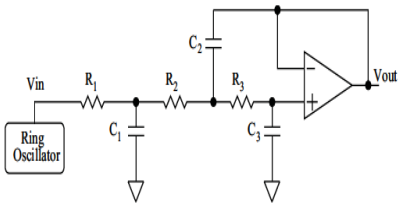

Figure.3 Active low pass Sallen–Key filter circuit. No dc current path exists between the input and output nodes

For a voltage regulator, the on-chip area requirement, sensitivity of the active filter to component parameter variations (due to aging, temperature, and process variations), and the power dissipated by the active components should be low. Two topologies are popular for implementing an integrated low pass active filter, i.e., multiple feedback and Sallen–Key [20]. Multiple feedback low pass filters use capacitive and resistive components within the feedback path from the output to the input. They are less suitable for an active filter-based on-chip voltage regulator. Alternatively, Sallen–Key low pass filters use only capacitive feedback. Hence, the static power dissipation of the Sallen–Key topology is significantly less than that in the multiple feedback topology.

A third order low pass unity gain Sallen–Key filter topology is shown in Figure. 3. The first section, R1 and C1, forms a first order low pass RC filter. The remaining components, i.e., R2, R3, C2, C3, and the Op Amp, form a second order Sallen–Key low pass filter. Note that no dc current path exists between the input and output. The gain of the active filter can be increased by inserting resistive feedback between the non inverting input and output nodes, forming a dc current path between the output and ground. Since low power dissipation is crucial to the proposed circuit, a unity gain topology is chosen.

$$\frac{Vout}{Vin} = \frac{1}{a1\ s3 + a2\ s2 + a3\ s + a4}$$

where
a1 = R1R2R3C1C2C3,
a2 = R1C1C3(R2 + R3) + R3C2C3(R1 + R2),
a3 = R1C1 + C3(R1 + R2 + R3),
a4 = 1

A Chebyshev type I filter is chosen for the active filter because of the steep roll-off factor as compared to the filter structures that do not require resistive components connected to ground to produce finite zeros. The active filter passes the switching signal at a constant frequency and generates a dc output voltage. A third order Chebyshev type I low pass Sallen–Key filter, shown in Figure. 3, is utilized in the proposed voltage regulator since no attenuation occurs at dc when the order of the Chebyshev filter is odd.

B. Op-Amp

The performance of an active filter depends strongly on the Op Amp. The gain–bandwidth product of the Op Amp determines the bandwidth of the active filter. Most of the power loss takes place within the Op Amp structure, since the current provided to the output load is supplied by the Op Amp output stage. Hence, the Op Amp needs to provide tens of milliamps of current to the load devices while maintaining sufficient performance to reliably operate the active filter. A three stage classical differential-input single-ended CMOS Op Amp structure is utilized in the proposed regulator, as shown in Figure. 4 [22]. The size of transistors in the output stage is considerably larger than the first two stages to supply sufficient current to the load circuits.

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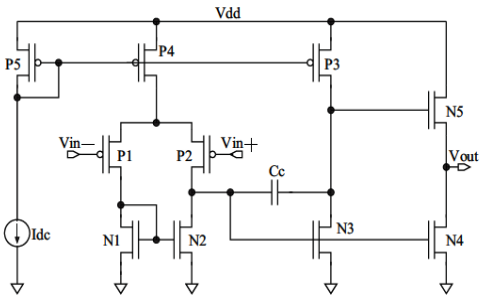
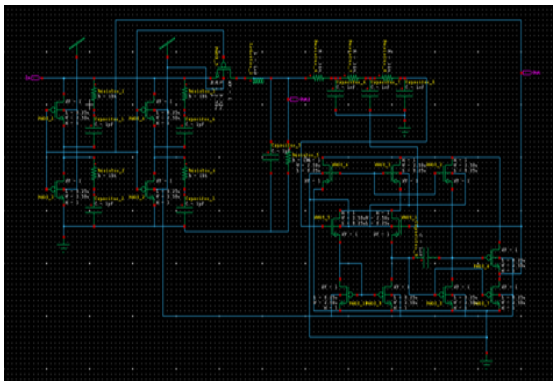
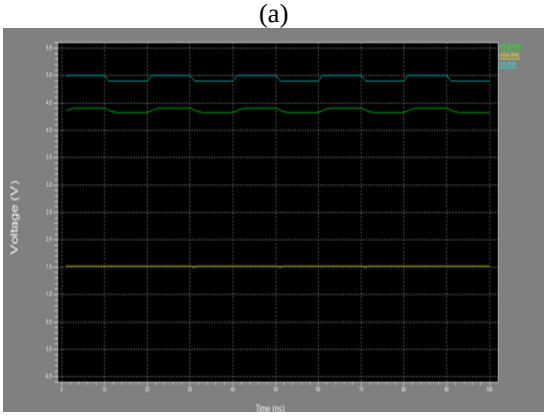


Figure.4 Three stage Op Amp with PMOS input transistors. The PMOS input transistors are used in the first differential input stage. The second stage is a common-source gain stage and the third stage forms the output buffer that supplies the current to the load.



(a)



(b)

Figure.5 (a) Schematic diagram of proposed DC-DC converter with active filter circuit and (b) Simulation result of proposed DC-DC converter

Figure.5 shows the schematic diagram of entire proposed circuit, where the passive LC filter is replaced with an active filter and large tapered buffers are no longer necessary. Since no direct current can be given to the bridged buck converter so the resistors and capacitors are used to overcome this problem. The input voltage signal is given at Vin and step down output is obtained at out2. Figure.6 shows the simulation result of DC-DC converter, where the out2 represents step down voltage of input signal and out represents the noise signal which is minimized to lower value. The table-I represents the timing analysis of the converter with less transient response, overhead and total simulation time.

Table I Timing Analysis

Setup	0.01
DC operating point	0.01
Transient analysis	0.03
Overhead	1.56
Total simulation	1.63

Conclusion

In this paper we described the active filter based DC-DC buck converter and its performance analysis. The on-chip area for the proposed fully monolithic hybrid voltage regulator is about 0.015 mm^2. The area required for the proposed regulator is significantly less than that of previously proposed state-of-the-art buck converters, LDO, and SC voltage regulators. The area of the proposed regulator will therefore be significantly smaller with more advanced technologies. This circuit therefore provides a means for distributing multiple power supplies close to the load to reduce P/G noise while enhancing circuit performance by delivering a high quality supply voltage to the load circuitry. With the proposed voltage regulator, on chip signal and power integrity will be significantly enhanced with the capability of distributing multiple power supplies.

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